RAD750™ Radiation Hardened PowerPC™ Microprocessor

Richard Berger, David Artz, Paul Kapcio
Lockheed Martin Space Electronics & Communications

Abstract

The development of a high performance radiation hardened PowerPC microprocessor is nearing completion. The features of the RAD750 are described, as well as the process of radiation hardening the processor. The RAD750 product family includes a PCI support chip and a CompactPCI® 3U board, both of which are described.

Introduction

When it goes into production in early 2001, the RAD750 will be the highest performance radiation-hardened general-purpose processor available. A fully licensed circuit-by-circuit translation of the PowerPC 750™, the RAD750 provides the space community with commercial state of the art features and provides an order of magnitude increase in on-board processing capability compared to our industry leading current offering, the RAD6000™ [1]. Prototype hardware is expected in the 3rd quarter of 2000. The RAD750 CompactPCI single board computer, currently being developed by Lockheed Martin for JPL under the X2000 program, provides a modular standard product that allows the spacecraft developer excellent flexibility in system configuration.

RAD750 Features

The RAD750 is functionally identical to the PowerPC 750 (also known as the G3) that was announced in 1997 [2] and is being sold commercially in the current generation of Apple computers, as well as embedded VME and PCI processor boards. The RAD750 is expected to run at 166 MHz, providing a throughput of 300 Dhrystone MIPS, 7.2 SPECint95 and 4.3 SPECfp95. A 10-20% performance increase is possible via the addition of an external L2 cache chip.

The RAD750 is a superscalar RISC processor, with 6 execution units and a dispatch / completion system that allows out of order execution. Two instructions and a branch can be executed simultaneously. The RAD750 includes the all of the architectural enhancements added to the PowerPC 750. These include an integrated L2 cache controller with direct port to an optional 1MB external L2 cache, dual 8-way set associative 32KB L1 caches with Memory Management Units, hardware table logs for improved task switching performance, a branch history table and target cache for dynamic branch prediction, and dual fixed point execution units. The processor core is clocked at between 2X and 8X multiples (in ½ increments) of the system I/O bus, based on pin programmable settings. The L2 interface, controlled by a Delay Locked Loop, is clocked at ½ increments from full speed to 1/3 that of the processor core. A simplified block diagram of the RAD750 is shown in figure 1.

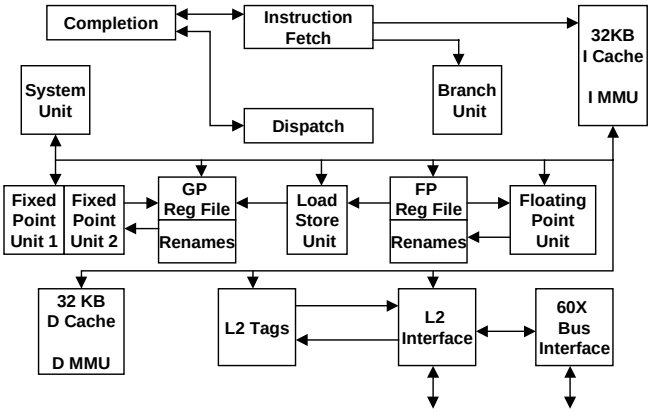

Figure 1. RAD750 Functional Block Diagram

The RAD750 supports a number of power management features, including both dynamic power management and multiple low power, limited function modes. Low speed full function operation is also possible with the RAD750, by bypassing the integrated Phase Locked Loop (PLL) and controlling the clock directly. This capability is fully supported by the Power PCI support chip.

The RAD750 core logic employs a 2.5 volt supply. The chip I/O circuits are designed to operate at either 2.5 or 3.3 volts.

Radiation Hardening the RAD750

The RAD750 translation started from the complete design database of the 0.18 micron version of the PowerPC 750. The RAD750 team has leveraged the data and methodology to increase productivity. The entire design is being replaced on a circuit by circuit basis, employing all three of the techniques employed in the original approach to optimize both power and performance. The control logic functions employ a high performance, low power standard cell library that reuses the Lockheed Martin 0.25 micron ASIC library. The high performance data flow found in areas such as the execution units employs a specialized circuit library that includes complex functions such as 32 bit incrementers, comparators, and rotators. Custom designed dynamic functions such as high speed adders used with the original data flow library, have been replaced by high performance static equivalent designs. The custom designed memory array and analog functions like the PLL have been redesigned as custom functions, with all of the dynamic logic

translated to high performance static logic. This includes replacement of dynamic logic functions such as address decoding, read-write control, and array data paths.

Given the high performance, the advanced small feature 0.25 micron lithography, the added complexity, and the PLL-based clocking of the RAD750, new techniques for radiation hardened circuit design were required to supplement those employed over the last decade. In addition, the desired portability of the RAD750 to commercial foundries provided the incentive to eliminate unique process steps. Research has been performed and published in this area [3].

There are over 800,000 storage elements in the PowerPC 750, all of which have been replaced with SEU hardened circuitry in the RAD750. The earlier RAD6000 employed resistivity hardened storage elements, requiring a special polysilicon resistor in the manufacturing process. The RAM cells and latches in the RAD750 have been designed using circuit hardening techniques that require no special process steps and optimize performance. These techniques have been developed and refined over a number of years. The effectiveness of these techniques in the 0.25 micron process was demonstrated on a technology test site in 1998 [4], and further enhanced since that time with an additional test site and a prototype 4 Mbit SRAM in 1999 [5]. Incorporating the knowledge gained from these earlier efforts, the RAD750 is expected to achieve SEU hardness levels of 1E-11 upsets/bit-day.

Recently, the contribution to Single Event Upsets from transients introduced in combinational logic has received increased attention [6]. Sometimes called Single Event Transients (SET), this effect may increase dramatically in high performance, small lithography designs. SET effects appear as pulses introduced to combinational logic functions as the result of a single event particle impact. An SET can propagate and eventually store in a storage element or introduce a spurious clock. Spurious clocks are particularly damaging to the dynamic logic often found in high performance designs. The RAD750 design employs techniques to mitigate SET induced upsets, through enhancements for pulse minimization and rejection.

The voltage controlled oscillator found in the PLL offered a special challenge. This circuitry has been hardened against SEU and SET effects, employing a newly developed circuit technique. Temperature compensation has also been added to support the full military temperature range.

The RAD750 die size is 120 square mm including the circuit designs optimized for the space environment. The RAD750 die is almost 20% smaller than the 145 square mm RAD6000 die, while incorporating an order of magnitude greater complexity. The original floorplan of the PowerPC 750 is also largely preserved in the RAD750, shown in figure 2.

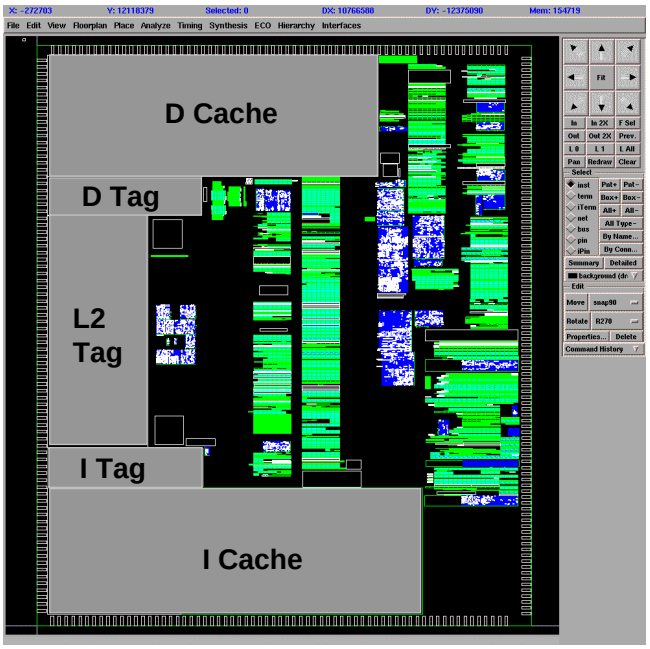

Figure 2. RAD750 Floorplan: October 1999

RAD750 Manufacturing Technology

The mainstream bulk 0.25 micron CMOS technology used for the RAD750 is being practiced by a number of commercial foundries with high volume, high reliability, and exceptional yields. The RAD750 prototype will be manufactured at one or more of these commercial foundries where this technology is considered mature. The technology features an Leff of 0.18 microns, supports up to six levels of metal interconnect with planarized passivation, and is designed for 2.5 volt operation. The technology has been tested and measured for Total Ionizing Dose, and has achieved levels of 200 Krad(Si).

The RAD750 is designed for manufacturability at multiple foundries. As such, one of the process features employed in the original PowerPC 750, tungsten local interconnect, has not been included on the RAD750. This decision was made due to the contribution of the local interconnect to device leakage and because it is not universally available. The L1 cache redundancy fuses have been retained.

The RAD750 will be packaged in a Ceramic Column Grid Array (CGA) package, constructed by attaching extended columns to the original Ball Grid Array (BGA) 360 pin package employed for the 0.25 micron PowerPC 750. The CGA package has been adopted

because it is better suited to the stresses of launch and the space environment [7]. The CGA has demonstrated significantly increased reliability during temperature cycling and stress, when compared to BGA packages, as shown in Figure 3. The CGA package has also passed shock and vibration testing for the space launch environment. The CGA has been qualified, and has been analyzed by JPL. This approach has the advantage of pin for pin compatibility between the RAD750 and it's commercial equivalent, allowing direct replacement on the same circuit board.

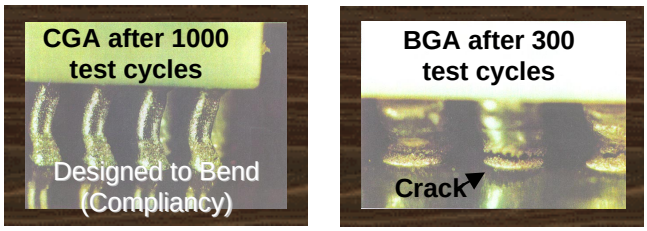

Figure 3. Package Reliability Comparison

Verification of the RAD750

The original design database of the PowerPC 750 used proprietary languages and data formats, which have now been translated to their COTS equivalents. The behavioral model of the full design has been coded in VHDL, and has been verified with the original PowerPC 750 validation test suite. This model is being used to provide test vectors for the individual subunits, to validate the translation and the replacement of dynamic circuitry.

Circuit level simulation is being performed on the custom array functions, employing the vectors generated with the behavioral model. Static timing analysis is being performed, using the static timing analysis results from the PowerPC 750 for reference. Formal verification is also being performed in a hierarchical fashion.

Verification of the RAD750 in conjunction with it's PCI support chip, called the Power PCI, is being performed by interlocking the VHDL models at the 60X system bus interface. This step is considered important to the verification of the Power PCI as well as the RAD750.

RAD750 System Architecture

The Power PCI Interface ASIC complements the RAD750 microprocessor chip. It provides the interface from the RAD750 to main memory and to the board or backplane 33 MHz 32 bit PCI bus (version 2.2). The Power PCI acts as the arbiter for the PCI bus, and the PCI bus is clocked asynchronously to the RAD750 interface. The Power PCI is based on reusable logic cores, coded in synthesizable VHDL. It employs two internal buses, one 64 bits wide and the other 32 bits wide, as well as a dedicated 64 bit bus between the processor interface and memory for high performance memory access. A block diagram of the Power PCI chip is shown in figure 4.

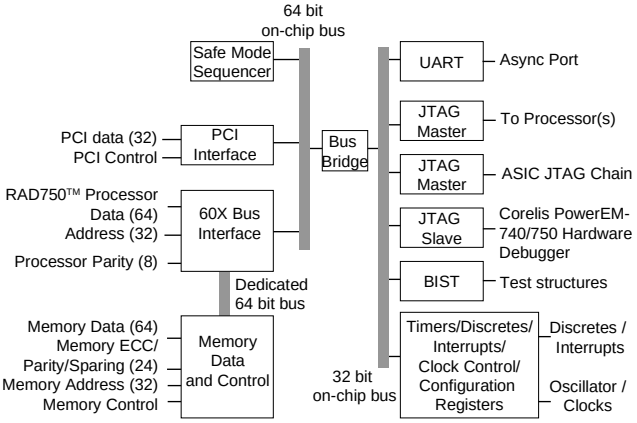

Figure 4. Power PCI Block Diagram

The Power PCI is neither pin compatible nor functionally identical to a commercial part because users in the space community required additional features and had different priorities than typical commercial customers. The Power PCI is designed to be as similar as possible to the most popular commercial bridge chip, the Motorola MPC-106, to preserve the basic programming interface, with the additional capability added as a superset of the design. For example, the Power PCI architecture optimizes error corrected memory performance, and adds nibble correction. It also adds an on-chip 16550 compatible UART, eliminating that board component's size and additional cost.

The Power PCI is manufactured on a 0.5 micron radiation hardened process line with 0.5 micron Leff and up to 5 levels of metal with planarized passivation. The technology will achieve Total Ionizing Dose hardness levels of 1 Mrad(Si). The ASIC library employed by this design has been proven on a number of designs, and has been tested for SEU to levels well beyond 1E-10 upsets/bit-day. The Power PCI chip requires a 3.3 volt supply.

The RAD750 CPU and Power PCI interface chips are designed to easily replace the RAD6000 CPU, the LIO interface chip, and the PMP interface chip within the current RAD6000 processor architecture [8]. The architectures use common software APIs, can employ common software tools, and use the WindRiver VxWorks Operating System. The Green Hills Multi compiler supports both processors, converting most code directly. Even machine language code will require only minor updates. These attributes combine to make the RAD6000 to RAD750 transition as easy as possible.

In addition to the Power PCI, the RAD750 family includes a CompactPCI 3U format single board computer, shown below in figure 5.

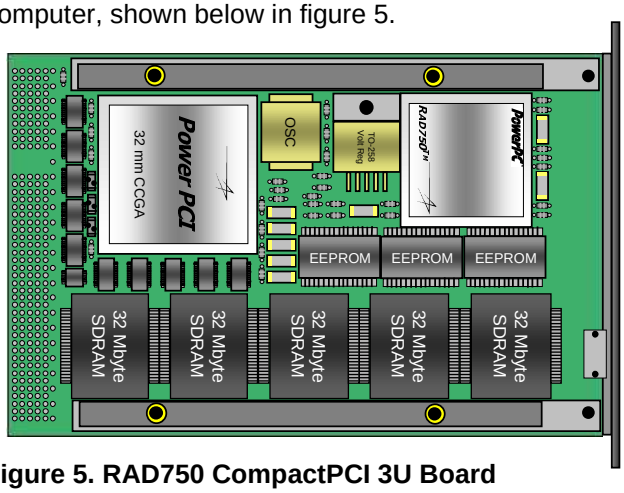

Figure 5. RAD750 CompactPCI 3U Board

This single board computer consists of the two new chips as well as 128 MB of synchronous DRAM packaged in 4 high stacks and 256 KB of EEPROM, both with error correction. An on-board regulator generates the 2.5 volts required for the RAD750 processor core, so the board only requires a 3.3 volt supply. The compact size of the 3U board provides greater flexibility in spacecraft size and shape, and is well suited to modular design of systems based on standard products, lowering costs and improving turn around time when compared to the typical custom board approach found with larger formats. The RAD750 CompactPCI board is offered as a standard product, provided with an accompanying board support package. Additional board variations may be provided in the future, based on customer demand.

The RAD750, like the PowerPC 750, is supported by a massive variety of commercially available operating systems and compilers. The original testing of the RAD750 board is being performed with WindRiver's Tornado environment. The debug environment employs the Corelis PowerEM-740/750 Hardware Debugger, a commercially available, PC-based product with in circuit emulation capability.

Information concerning the RAD750 is available through the RAD750 web site. Customer support for the RAD750 will be available via the web site, a dedicated e-mail address, and an 800 number [9].

Summary

The RAD750 CPU represents a new generation of spaceborne processor, with an order of magnitude increase in performance over the currently available products. The RAD750 is designed for production using commercial foundries, yet provides excellent radiation hardened characteristics. The complete RAD750 processor architecture provides for easy migration for users of the current RAD6000 family of products, and for modular system construction. The RAD750 family of products is a complete solution for the space community.

Acknowledgements

The authors wish to thank the members of the RAD750 design team, the PowerPC 750 design team, the Power PCI and CompactPCI board design teams, as well as JPL and AFRL for their support.

References

[1] R. Kettlekamp, et al.; "Radiation Hardened 32-bit RISC Microprocessor for Space", 1997 GOMAC Conference Proceedings, Volume XXII, March 1997

[2] G. Gerosa, et al.; "A 250 MHz 5-W PowerPC Microprocessor with On-Chip L2 Cache Controller", IEEE Journal of Solid State Circuits, Vol. 32, No 11, November 1997

[3] M. Norley Liu, et al. "Low Power SEU Immune CMOS Memory Circuits", IEEE Transactions on Nuclear Science, Vol. 39, No 6, December 1992

[4] A. Brown, et al.; "An Initial Evaluation of Lockheed Martin's 0.25µm CMOS Technology", 1999 GOMAC Conference Proceedings, Volume XXIV, March 1999

[5] J. Yoder, et al.; "Lockheed Martin Deep Submicron Efforts", 2000 GOMAC Conference Proceedings, Volume XXIV, March 2000

[6] K. Hass, et al.; "Mitigating Single Event Upsets From Combinational Logic", 7th NASA Symposium on VLSI Design 1998

[7] J. Hughes et al.; "Development of Surface Mount Solder Column Array Components for Advanced Packaging Satellite Applications", 1999 GOMAC Conference Proceedings, Volume XXIV, March 1999

[8] J. Marshall; "Dynamic Space Processor Architecture Built on Commercial Open System Interface Standards", 18th Digital Avionics Systems Conference Proceedings, October 1999

[9] Web site URL: www.RAD750.com; phone: 1-800-RAD750s; email: lm.rad750 @ lmco.com